**ARMv8 and RISC-V axiomatic memory models**

*arch* switches between ARMv8 and RISC-V.

let $obs = rfe \mid fr \mid co$
let $dob = addr \mid data$
$\quad \mid (addr \mid data); rfi$
$\quad \mid (ctrl \mid addr); po; [W]$
$\quad \mid (ctrl \mid addr); po; [\texttt{isb}]; po; [R]$
let $aob = [range(rmw)]; rfi; (if\ arch = \text{RISC-V}\ then\ R\ else\ [A|Q])$
let $bob = [R]; po; [\texttt{dmb.rr}]; po; [R]$
$\quad \mid [R]; po; [\texttt{dmb.rw}]; po; [W]$
$\quad \mid [W]; po; [\texttt{dmb.wr}]; po; [R]$
$\quad \mid [W]; po; [\texttt{dmb.ww}]; po; [W]$
$\quad \mid [L]; po; [A]$
$\quad \mid [A|Q]; po$
$\quad \mid po; [L]$
$\quad \mid if\ arch = \text{RISC-V}\ then\ rmw$
let $ob = obs \mid dob \mid aob \mid bob$
acyclic $po\text{-}loc \mid fr \mid co \mid rf$ as *internal*
acyclic $ob$ as *external*
empty $rmw \,\&\, (fre; coe)$ as *atomic*

The barriers here are `dmb.rw`, `dmb.rr`, `dmb.wr`, `dmb.ww`. All others are just combinations of these, for example: ARMv8's `dmb.ld` = `dmb.rw`; `dmb.rr`.